Amendments to the Claims:

Cancel claims 1-10.

11 A memory device for communicating with an integrated circuit via a communication bus, said device comprising:

an interface circuit for receiving communication signals from the communication bus, and for decoding the communication signals, and for generating a plurality of protocol signals;

a multiplexer for receiving the plurality of protocol signals and for outputting one of the plurality of protocol signals corresponding to a one protocol in response to a select signal;

a user selectable non-volatile memory for storing user input representative of the one protocol and for generating the select signal;

a non-volatile memory; and

a controller for controlling the non-volatile memory; said controller responsive to said select signal;

wherein upon storing the user input, the memory device is responsive to communication signals only in the one protocol.

12. The memory device of claim 11 wherein the plurality of protocol signals represent protocol for LPC communication, FWH communication.

13. The memory device of claim 11 wherein the user selectable non-volatile memory comprises a non-volatile fuse.

14. The memory device of claim 13 further comprising:

a programming logic circuit for receiving the user selected protocol to program the non-volatile fuse.

15. The memory device of claim 14 further comprising:

said non-volatile fuse has an output;

a fuse sense circuit for receiving the output and for generating a fuse control signal;

a latch for receiving the fuse control circuit and for generating the select signal.

16. The memory device of claim 15 further comprising:

a mode selecting-circuit responsive to a test signal for testing the memory device or for operating the memory device.

17. The memory device of claim 11 wherein said user selectable non-volatile memory further comprising:

a non-volatile memory for storing the user input;

a sensor for receiving the output of the non-volatile memory and for generating the select signal.

18. A configurable memory controller for controlling a memory, comprising:

a decoder circuit for receiving communication signals from a communication bus, and for decoding the communication signals and for generating a plurality of protocol signals;

a non-volatile memory for storing user input representative of one protocol; said non-volatile memory having an output;

a sensing circuit for receiving the output of the non-volatile memory and for generating a select signal;

a multiplexer for receiving the select signal and the plurality of protocol signals from the decoder circuit and for outputting a select protocol signal in response to the select signal; wherein the select protocol signal is representative of the one protocol; and

a controller for receiving the select signal and the select protocol signal for controlling the memory.

19. The memory controller of claim 18, wherein the plurality of protocol signals represent protocol for LPC communication, FWH communication.

20. A memory device for receiving communication signals from a communication bus, comprising;

a decoding circuit connected to the communication bus for receiving the communication signals and for generating a protocol select signal;

a first non-volatile memory for storing the protocol select signal;

a delay circuit connected to the communication bus for receiving the communication signals and for generating a delayed communication signal;

a second non-volatile memory; and

a controller for receiving the delayed communication signal and the protocol select signal, and for controlling the operation of the second non-volatile memory in response to the delayed communication signal as selected by the protocol select signal.